What Is Claimed Is:

1. A manufacturing method of a thin film transistor (TFT), comprising the steps of:

providing a substrate;

depositing a conductive layer above the substrate to form a gate electrode of the thin film transistor;

forming an insulating layer above the conductive layer and the substrate;

sequentially forming a semiconductor layer and a doped silicon layer on the insulating layer;

depositing a sacrifice layer with an island shape above the doped silicon layer, and the sacrifice layer being positioned directly above the gate electrode;

forming a metal layer covering the sacrifice layer and the doped silicon layer;

patterning the metal layer to form a source electrode and a drain electrode, a channel being defined between the source electrode and the drain electrode, a non-TFT region being defined as a portion of the substrate not covered by the source electrode, the drain electrode, and the channel, and the island-shaped sacrifice layer being exposed in the channel and the doped silicon layer being exposed in the non-TFT region after the metal layer being patterned;

using the source and the drain electrodes as a mask to perform the following etching processes in the same time during a predetermined period: (a) removing the island-shaped sacrifice layer and the doped silicon layer in the channel so that the semiconductor layer being exposed in the channel; and (b) removing

the doped silicon layer and the semiconductor layer in the non-TFT region to expose the insulating layer; and

forming a passivation layer to cover the source electrode, the drain electrode, the channel, and the substrate.

2. The method of claim 1, wherein during the etching process, etching rates and the thickness of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are respectively R_{IS}, T_{IS}, R_n, T_n, R_a, and T_a, and the time for removing the island-shaped sacrifice layer and the doped silicon layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is not less than the time for removing the doped silicon layer and the semiconductor layer in the non-TFT region ($T_n/R_n + T_a/R_a$).

3. The method of claim 2, wherein the thickness of the insulating layer in the non-TFT region is reduced by controlling the thickness of the island-shaped sacrifice layer so that a portion of the insulating layer is removed in the non-TFT region when the island-shaped sacrifice layer and the doped silicon layer is removed in the channel, and the doped silicon layer and the semiconductor layer is removed in the non-TFT region.

4. The method of claim 3, wherein the etching rate and the thickness of the removed insulating layer is R_{INS} and T_{INS}, and the time for removing the sacrifice layer and the doped silicon layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is equal to the time for removing the doped silicon layer, the semiconductor layer and the removed insulating layer in the non-TFT region ($T_n/R_n + T_a/R_a + T_{INS}/R_{INS}$).

5. The method of claim 1, further comprising the following steps:

etching the passivation layer to expose one of the source electrode and the drain electrode; and

forming a transparent conductive layer above the passivation layer so as to electrically connect to one of the source electrode and the drain electrode.

6. The method of claim 5, wherein the semiconductor layer is an amorphous silicon layer, the doped silicon layer is an n-type poly-silicon layer, the conductive layer is a metal layer, the substrate is made of glass or quartz, and the transparent conductive layer is an indium tin oxide (ITO) layer.

7. A method for manufacturing a thin film transistor (TFT), comprising the steps of:

providing a substrate;

depositing a conductive layer above the substrate to form a gate electrode of the thin film transistor;

forming an insulating layer above the conductive layer and the substrate;

forming a semiconductor layer on the insulating layer;

forming a sacrifice layer with an island shape on the semiconductor layer, and the sacrifice layer being positioned directly above the gate electrode;

forming a doped silicon layer on the sacrifice layer and the semiconductor layer;

forming a metal layer covering the doped silicon layer;

patterning the metal layer to form a source electrode and a drain electrode, a channel being defined between the source

electrode and the drain electrode, a non-TFT region being defined as a portion of the substrate not covered by the source electrode, the drain electrode and the channel, and the doped silicon layer being exposed in the channel and the non-TFT region;

using the source and the drain electrodes as a mask to perform the following etching processes at the same time during a predetermined period: (a) removing the doped silicon layer and the island-shaped sacrifice layer within the channel so as to expose the semiconductor layer in the channel; and (b) removing the doped silicon layer and the semiconductor layer in the non-TFT region so as to expose the insulating layer; and

forming a passivation layer to cover the source electrode, the drain electrode, the channel, and the non-TFT region.

8. The method of claim 7, wherein during the etching process, the etching rate and the thickness of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are respectively R_{IS}, T_{IS}, R_n, T_n, R_a, and T_a, and the time for removing the doped silicon layer and the island-shaped sacrifice layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is not less than the time for removing the doped silicon layer and the semiconductor layer in the non-TFT region ($T_n/R_n + T_a/R_a$).

9. The method of claim 8, wherein the thickness of the insulating layer in the non-TFT region is reduced by controlling the thickness of the island-shaped sacrifice layer so that a portion of the insulating layer is removed in the non-TFT region when the doped silicon layer and the island-shaped sacrifice layer is etched in the channel.

10. The method of claim 9, wherein the etching rate and the thickness of the removed insulating layer are respectively R_{INS} and T_{INS}, the time for removing the doped silicon layer and the island-shaped sacrifice layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is equal to the time for removing the doped silicon layer, the semiconductor layer, and the removed insulating layer in the non-TFT region ($T_n/R_n + T_a/R_a + T_{INS}/R_{INS}$).

11. The method of claim 7, further comprising the following steps:

etching the passivation layer to expose one of the source electrode and the drain electrode; and

forming a transparent conductive layer above the passivation layer so as to electrically connect to one of the source electrode and the drain electrode.

12. The method of claim 11, wherein the semiconductor layer is an amorphous silicon layer, the doped silicon layer is an n-type poly-silicon layer, the conductive layer is a metal layer, and the transparent conductive layer is an ITO layer.

13. A method for forming a thin film transistor liquid crystal display (TFT-LCD), the TFT-LCD including at least one thin film transistor (TFT) and one storage capacitor (Cs), the method comprising the steps of:

providing a substrate;

depositing a first and a second conductive layer on the substrate to form a gate electrode of the TFT and a bottom electrode of the storage capacitor and ;

forming an insulating layer above the conductive layers and the substrate;

sequentially forming a semiconductor layer and a doped silicon layer on the insulating layer;

depositing a sacrifice layer with an island shape above the doped silicon layer, and the sacrifice layer being positioned directly above the first conductive layer;

forming a metal layer covering the sacrifice layer and the doped silicon layer;

patterning the metal layer to form a source electrode and a drain electrode above the first conductive layer, a channel being defined between the source electrode and the drain electrode to expose the sacrifice layer therein, and a non-TFT region being defined as a portion of the substrate not covered by the source electrode, the drain electrode, and the channel so as to expose the doped silicon layer thereon;

using the source and the drain electrodes as a mask to perform the following etching processes at the same time (a) to remove the island-shaped sacrifice layer and the doped silicon layer in the channel, as well as (b) to remove the doped silicon layer and the semiconductor layer in the non-TFT region, so that the semiconductor layer being exposed in the channel and the insulating layer being exposed in the non-TFT region; and

forming a passivation layer to cover the source electrode, the drain electrode, the channel, and the second conductive layer.

14. The method of claim 13, wherein during the etching process, etching rates of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are respectively R_{IS},

R_n and R_a, the thickness of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are respectively T_{IS}, T_n, and T_a, and the time for removing the island-shaped sacrifice layer and the doped silicon layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is not less than the time for removing the doped silicon layer and the semiconductor layer in the non-TFT region ($T_n/R_n + T_a/R_a$).

15. The method of claim 14, wherein the thickness of the insulating layer in the non-TFT region is reduced by controlling the thickness of the island-shaped sacrifice layer so that a portion of the insulating layer is removed in the non-TFT region when the island-shaped sacrifice layer and the doped silicon layer is removed in the channel, and the doped silicon layer and the semiconductor layer is removed in the non-TFT region.

16. The method of claim 15, wherein the etching rate and the thickness of the removed insulating layer are R_{INS} and T_{INS}, and the time for removing the island-shaped sacrifice layer and the doped silicon layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is equal to the time for removing the doped silicon layer, the semiconductor layer, and the removed insulating layer in the non-TFT region ($T_n/R_n + T_a/R_a + T_{INS}/R_{INS}$).

17. The method of claim 13, further comprising the following steps:

forming a hole in the passivation layer to expose one of the source electrode and the drain electrode; and

depositing a transparent conductive layer above the passivation layer and extending above one of the source and drain

electrodes and the second conductive layer, and the transparent conductive layer being electrically connected to one of the source and drain electrodes through the hole for forming an upper electrode of the storage capacitor.

18. A method for forming a thin film transistor liquid crystal display (TFT-LCD), the TFT-LCD having at least one thin film transistor (TFT) and one storage capacitor (Cs), the method comprising the steps of:

providing a substrate;

depositing a first conductive layer and a second conductive layer above the substrate to form a gate electrode of the TFT and a bottom electrode of the storage capacitor;

forming an insulating layer on the first and second conductive layers and the substrate;

depositing a semiconductor layer and a doped silicon layer on the insulating layer;

forming a sacrifice layer with an island shape on the doped silicon layer, and the sacrifice layer being positioned directly above the first conductive layer;

forming a metal layer covering the sacrifice layer and the doped silicon layer;

patterning the metal layer to form a source electrode and a drain electrode above the first conductive layer as well as to form a shielding metal layer above the second conductive layer, a channel being defined between the source electrode and the drain electrode to expose the sacrifice layer in the channel, a capacitor region being defined as a portion of the substrate covered by the shielding metal layer, and a non-TFT region being defined as a portion of the substrate not covered by the source

electrode, the drain electrode, the capacitor region, and the channel so as to exposed the doped silicon layer thereon;

using the source electrode, the drain electrode, and the shielding metal layer as a mask to perform the following etching processes at the same time: (a) removing the doped silicon layer and the island-shaped sacrifice layer in the channel so as to expose the semiconductor layer therein, and (b) removing the doped silicon layer and the semiconductor layer in the non-TFT region so as to expose the insulating layer thereon; and

forming a passivation layer to cover the source electrode, the drain electrode, the channel, and the capacitor region.

19. The method of claim 18, wherein during the etching process, etching rates of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are R_{IS}, R_n, and R_a respectively, the thickness of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are T_{IS}, T_n, and T_a, and the time for removing the island-shaped sacrifice layer and the doped silicon layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is not less than the time for removing the doped silicon layer and the semiconductor layer in the non-TFT region ($T_n/R_n + T_a/R_a$).

20. The method of claim 18 further comprising the following steps:

patterning the passivation layer to form a first hole and a second hole so as to expose one of the source electrode and the drain electrode through the first hole, and expose the shielding metal layer in the capacitor region through the second hole; and

forming a transparent conductive layer above the passivation layer, the transparent conductive layer being electrically connected to one of the source and the drain electrodes through the first hole, as well as electrically connected to the shielding metal layer through the second hole for forming an upper electrode of the storage capacitor.

21. A method for manufacturing a thin film transistor liquid crystal display (TFT-LCD), the TFT-LCD having at least one thin film transistor (TFT) and one storage capacitor (Cs), the method comprising the steps of:

providing a substrate;

depositing a first and a second conductive layer above the substrate to form a gate electrode of the TFT and a bottom electrode of the storage capacitor, respectively;

forming an insulating layer above the conductive layers and the substrate;

depositing a semiconductor layer on the insulating layer;

forming a sacrifice layer with an island shape on the semiconductor layer, and the sacrifice layer being positioned directly above the first conductive layer;

depositing a doped silicon layer on the island-shaped sacrifice layer and the semiconductor layer;

forming a metal layer covering the doped silicon layer and the island-shaped sacrifice layer;

patterning the metal layer to form a source electrode and a drain electrode above the first conductive layer, a channel being defined between the source electrode and the drain electrode to expose the doped silicon layer therein, and a non-FT region being defined as a portion of the substrate not covered

by the source electrode, the drain electrode, and the channel to expose the doped silicon layer thereon;

using the source and the drain electrodes as a mask to perform the following etching processes at the same time to (a) remove the doped silicon layer and the island-shaped sacrifice layer in the channel so as to expose the semiconductor layer in the channel, and (b) to remove the doped silicon layer and the semiconductor layer in the non-TFT region so as to expose the insulating layer; and

forming a passivation layer to cover the source electrode, the drain electrode, the channel, and the second conductive layer.

22. The method of claim 21, wherein during the etching process, the etching rate and the thickness of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are R_{IS}, T_{IS}, R_n, T_n, R_a, and T_a respectively; and the time for removing the doped silicon layer and the island-shaped sacrifice layer in the channel $(T_{IS}/R_{IS} + T_n/R_n)$ is not less than the time for removing the doped silicon layer and the semiconductor layer in the non-TFT region $(T_n/R_n + T_a/R_a)$.

23. The method of claim 22, wherein the thickness of the insulating layer in the non-TFT is reduced by controlling the thickness of the island-shaped sacrifice layer so that a portion of the insulating layer is removed in the non-TFT region when the doped silicon layer and the island-shaped sacrifice layer in the channel is etched away.

24. The method of claim 23, wherein the etching rate and the thickness of the removed insulating layer are R_{INS} and T_{INS}, and the time for removing the doped silicon layer and the island-shaped sacrifice layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is equal to the time for removing the doped silicon layer, the semiconductor layer, and the removed insulating layer in the non-TFT region ($T_n/R_n + T_a/R_a + T_{INS}/R_{INS}$).

25. The method of claim 21 further comprising the following steps:

forming a hole in the passivation layer to expose one of the source and drain electrodes; and

depositing a transparent conductive layer above the passivation layer so as to electrically connect to one of the source and drain electrodes through the hole.

26. A method for manufacturing a thin film transistor liquid crystal display (TFT-LCD), the TFT-LCD having at least one thin film transistor (TFT) and one storage capacitor, the method comprising the steps of:

providing a substrate;

depositing first and second conductive layers above the substrate to respectively form a gate electrode of the TFT and a bottom electrode of the storage capacitor;

forming an insulating layer above the first and second conductive layers and the substrate;

forming a semiconductor layer on the insulating layer;

forming a sacrifice layer with an island shape on the semiconductor layer, and the sacrifice layer being positioned directly above the first conductive layer;

depositing a doped silicon layer to cover the sacrifice layer and the semiconductor layer;

forming a metal layer covering the doped silicon layer;

patterning the metal layer to form a source electrode and a drain electrode above the first conductive layer, as well as to form a shielding metal layer above the second conductive layer; a channel being defined between the source electrode and the drain electrode to expose the doped silicon layer therein; a capacitor region being defined as a portion of the substrate covered by the shielding metal layer; and a non-TFT region being defined as the substrate not covered by the source electrode, the drain electrode, the capacitor, and the channel so as to expose the doped silicon layer thereon;

using the source and drain electrodes and the shielding metal layer as a mask to perform these etching processes at the same time: (a) removing the doped silicon layer and the island-shaped sacrifice layer in the channel so as to expose the semiconductor layer in the channel, and (b) removing the doped silicon and semiconductor layers in the non-TFT region to expose the insulating layer therein; and

forming a passivation layer to cover the source electrode, the drain electrode, the channel, and the capacitor region.

27. The method of claim 26, wherein during the etching process, etching rates of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are R_{IS}, R_n, and R_a respectively; the thickness of the island-shaped sacrifice layer, the doped silicon layer, and the semiconductor layer are T_{IS}, T_n, and T_a; and the time for removing the doped silicon layer and the island-shaped sacrifice layer in the channel (T_{IS}/R_{IS} +

T_n/R_n) is not less than the time for removing the doped silicon layer and the semiconductor layer in the non-TFT region ($T_n/R_n + T_a/R_a$).

28. The method of claim 27 further comprising the following steps:

forming a first hole and a second hole in the passivation layer so as to expose one of the source and drain electrodes via the first hole, and expose the shielding metal layer via the second hole; and

forming a transparent conductive layer above the passivation layer, the transparent conductive layer being electrically connected to one of the source electrode and the drain electrode through the first hole, as well as electrically connected to the shielding metal through the second hole for forming an upper electrode of the storage capacitor.

29. A thin film transistor (TFT), comprising:

a gate electrode with an island shape formed on a substrate;

an insulating layer covering the gate electrode;

a semiconductor layer with an island shape formed on the insulating layer, and positioned directly above the gate electrode;

a source doped silicon layer and a drain doped silicon layer formed on the semiconductor layer, a channel being defined between the source doped silicon layer and the drain doped silicon layer to expose the semiconductor layer therein;

first and second sacrifice layers with island shapes respectively formed on the source doped silicon layer and drain

doped silicon layer, the first and the second sacrifice layers being spaced apart by the channel;

a source electrode formed above the first sacrifice layer and the source dope silicon layer; and

a drain electrode formed above the second sacrifice layer and the drain doped silicon layer;

wherein the thickness of the first and second sacrifice layers varies according to the thickness of the semiconductor layer because the time for etching the first and second sacrifice layers is substantially equal to the time for etching the semiconductor layer in the subsequent process.

30. The TFT in claim 29, wherein during the etching process, the etching rate of the first and the second sacrifice layers is R_{IS}, the etching rate and the thickness of the drain doped silicon and the source doped silicon layers are R_n and T_n, and the etching rate and the thickness of the semiconductor layer are R_a and T_a, and the thickness of the first and the second sacrifice layers T_{IS} meets the equation of $(T_{IS}/R_{IS} + T_n/R_n) \geqq (T_n/R_n + T_a/R_a)$.

31. The TFT in claim 29, further comprising a passivation layer covering the source electrode, the drain electrode, and the channel, and the TFT is used in an in-plane-switch (IPS) type LCD.

32. The TFT in claim 29, further comprising:

a passivation layer covering the TFT on the substrate, and having a hole above the drain electrode; and

a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole.

33. A thin film transistor (TFT), comprising:

a gate electrode with an island shape formed on a substrate;

an insulating layer covering the gate electrode;

a semiconductor layer with an island shape formed on the insulating layer, and positioned above the gate electrode;

first and second sacrifice layers with island shapes formed on the semiconductor layer, and a channel being defined between the first and second sacrifice layers so as to expose the semiconductor layer;

a source doped silicon layer and a drain doped silicon layer formed above the first sacrifice layer, second sacrifice layer, and the semiconductor layer, the source doped silicon layer and the drain doped silicon layer being spaced apart by the channel; and

a source electrode and a drain electrode respectively formed on the source doped silicon layer and the drain doped silicon layer;

wherein the thickness of the first and second sacrifice layers varies with the thickness of the semiconductor layer because the time for etching the first and second sacrifice layers is substantially equal to the time for etching the semiconductor layer in the subsequent process.

34. The TFT in claim 33, wherein the etching rate of the first and the second island-shaped sacrifice layers is R_{IS}, the etching rate and the thickness of the drain doped silicon and the source doped silicon layers are R_n and T_n, the etching rate and the thickness of the island-shaped semiconductor layer are R_a and T_a, and the thickness of the first and the second island-like

sacrifice layers T_{IS} meets the equation of $(T_{IS}/R_{IS} + T_n/R_n) \geqq (T_n/R_n + T_a/R_a)$.

35. The TFT in claim 33, further comprising a passivation layer covering the source electrode, the drain electrode, and the channel, and the TFT is used in an in-plane-switch (IPS) type LCD.

36. The TFT in claim 33 further comprising:

a passivation layer covering the TFT on the substrate, and having a hole above the drain electrode; and

a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole.